REMARKS

Claims 1 and 3-23 are currently pending in the subject application and are presently under consideration. Claims 1, 3, 4, 5, 7, 9, 15-17 and 22 have been amended herein. Claim 9 and 15 have been amended to remove trademark names. A listing of all claims is at pages 2-5.

Favorable reconsideration of the subject patent application is respectfully requested in view of the comments and amendments herein.

I. Rejection of Claims 1-8, 10, and 17-23 Under 35 U.S.C. §103(a)

Claims 1-8, 10, and 17-23, are rejected under 35 U.S.C. §103(a), as being unpatentable over U.S. 6,650,422 (Singh *et al.* '422) in view of U.S. 6,561,706 (Singh *et al.* '706) and US 6,905,949 (Arita). It is respectfully submitted that this rejection should be withdrawn for at least the following reasons. Singh *et al.* '422, Singh *et al.* '706 and Arita, alone or in combination, fail to teach or suggest each and every feature of the subject claims. In addition, the Examiner has not provided proper motivation to combine the teachings of Singh *et al.* '422, Singh *et al.* '706 and Arita.

> To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) *must teach or suggest all the claim limitations.* *See* MPEP §706.02(j). The *teaching or suggestion to make the claimed combination* and the reasonable expectation of success *must be found in the prior art and not based on the Applicant's disclosure.* *See In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). An *examiner cannot establish obviousness* by locating references which describe various aspects of a patent applicant's invention *without also providing evidence of the motivating force* which would impel one skilled in the art to do what the patent applicant has done. *Ex parte Levengod*, 28 USPQ2d 1300 (P.T.O.B.A.&I. 1993).

Applicants' invention relates generally to photolithographic systems and methods, and more particularly to systems and methods that facilitate monitoring and mitigating line-edge roughness and maintaining critical dimensions during gate formation in an integrated circuit. Independent claims 1, 10, and 17 recite similar limitations regarding a system and method that monitors information associated with ... critical dimensions ... line-edge roughness and non-lithographic shrink techniques that mitigate line-edge roughness if it exists and trim etch techniques that facilitate achieving objective critical dimensions in gate formation on semiconductors. Independent claim 1 as amended recites a system for ***mitigating line-edge roughness on a semiconductor device comprising...a monitoring component...a non-lithographic shrink component and...a trim etch component ... to achieve a target critical dimension***. Independent claim 10 recites a method for mitigating line-edge roughness on a semiconductor device, comprising, ***determining whether line-edge roughness exists on a patterned photoresist, employing a non-lithographic shrink technique to mitigate line-edge roughness, and employing a trim etch technique to compensate for any increase in critical dimension*** between lines on a photoresist. Independent 17 as amended recites a system for ***monitoring and mitigating line-edge roughness and trimming excess resist material to achieve a desired critical dimension***. Neither Singh *et al.* '422, Singh *et al.* '706 and Arita, alone or when combined, teach or suggest these novel features of applicants' claimed invention.

Singh *et al.* '422 discloses a system for *detecting asymmetry in a planar surface* based on the measurement of variation in the polarization of light after reflection off a plane surface. (*See* col. 4, lines 23-27, Figs. 2a-2e). The cited reference deals with a method to determine *angular asymmetry of a planar surface*, by directing a first and second beam of radiation at a first and second side, respectively, of a feature of the substrate and utilizing the reflected beams to determine the asymmetry. (*See* col. 2, lines 14-21, Fig. 2 and Figs. 2a-2e). Nowhere in Singh *et al.* '422 is it taught or suggested that the subject claims provide a system or method for mitigating line-edge roughness or trim techniques to maintain critical dimensions. Accordingly, Singh *et al.* '422 does not teach or suggest all of the claim limitations of the subject invention.

Moreover, the secondary document, Singh *et al.* '706, does not cure the aforementioned deficiency with respect to Singh *et al.* '422. Singh *et al.* '706 discloses "Monitoring and *controlling the exposure with runtime feedback provides superior exposure control and thus facilitates achieving desired critical dimensions*, with substantial uniformity in such critical

dimensions between layers. Similarly, *controlling subsequent manufacturing processes and/or apparatus based on data collected from monitoring a previous manufacturing process facilitates accounting for variations between wafers and/or variations between exposures*, which facilitates achieving desired critical dimensions." (*See* 2, ll. 30-39). However, like the primary document, Singh *et al.* '706, is silent with regard to a ***non-lithographic shrink component to mitigate line-edge roughness and trimming excess resist material to achieve a desired critical dimension***, rather Singh *et al.* '706 does not address line-edge roughness and achieves desired critical dimensions by *controlling the exposure of the photoresist in semiconductors* and not ***by trimming excess material*** on the current semiconductor.

Moreover, contrary to the Examiner's assertions, Singh *et al.* '422, Singh *et al.* '706 and Arita, alone or in combination, fail to teach or suggest all the features of the subject claims. Withdrawal of this rejection is respectfully requested for at least the following reasons. Arita *teaches a semiconductor apparatus fabrication method for suppressing edge roughness* when an extremely fine resist pattern is formed. Accordingly, Arita fails to teach or suggest a system for ***monitoring and mitigating line-edge roughness and trimming excess resist material.*** Rather in contrast to the claimed aspects, Arita teaches additional fabrication steps for suppressing line-edge roughness are performed on *every semiconductor and surface whether or not the fabrication steps are necessary*, whereas the subject claims provide a ***non-lithographic shrink component to mitigate line-edge roughness after the monitoring component reviews at least one critical dimension and line-edge roughness on a photoresist to determine of rework is required.*** In the claimed invention, if rework is not required, with regard to critical dimension or edge roughness, it is not performed.

Moreover, there is no teaching or suggestion to combine Singh *et al.* '422, Singh *et al.* '706 and Arita, as the Examiner suggests. While both cited references relate broadly to semiconductor manufacturing systems, Singh *et al.* '422 relates to a system for detecting asymmetry in a planar surface of a semiconductor based on measurement of variation in polarization of light after reflection on a plane surface and Singh *et al.* '706 relates to a post manufacturing process system that monitors dimensions of semiconductors to control the *exposure of photoresist in semiconductor fabrication*, to maintain critical dimensions. Arita is a secondary operation involving a semiconductor fabrication method that is used to reduce edge roughness on the entire semiconductor. There is no teaching, suggestion or motivation in the

references to modify Singh *et al.* '422 as suggested absent utilizing applicants' specification as a 20/20 hindsight based roadmap to provide the necessary motivation. The rationale proffered to modify Singh *et al.* '422 is to achieve benefits identified in applicants' specification rather than the cited references. Applicants' representative respectfully submits that this is an unacceptable and improper basis for a rejection under 35 U.S.C. 103. (*See Interconnect Planning Corporation v. Thomas E. Feil, Robert O. Carpenter, V Band Systems, Inc., and Turret Equipment Corp.*, 774 F.2d 1132, 1138 (Fed. Cir. 1985) (stating the invention must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time of the invention)). In essence, this rejection is based on an assertion that it would have been obvious to do something not suggested in the art because so doing would provide advantages stated in applicants' specification. This sort of rationale has been condemned by the Court of Appeals for the Federal Circuit. (*See Panduit Corp. v. Dennison Manufacturing Co.*, 1 USPQ2d 1593 (Fed. Cir. 1987)).

For at least the foregoing reasons, it is readily apparent that Singh *et al.* '422, Singh *et al.* '706 and Arita are not properly combinable. Even if they were properly combinable, Singh *et al.* '422, individually or in combination with Singh *et al.* '706 and Arita fail to teach or suggest all the limitations of the subject claims. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 2-8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Singh *et al.* '422, as applied to amended independent claim 1 above, and further in view of Singh *et al.* '706 and Arita. It is respectfully submitted that this rejection should be withdrawn for at least the following reasons. Neither Singh *et al.* '422 nor Singh *et al.* '706 and Arita, alone or in combination, teach or suggest all limitations recited in the subject claims.

Claim 2 has been canceled and claims 3-8 depend from independent claim 1 as amended above. As discussed *supra*, Singh *et al.* '422 does not teach or suggest all limitations recited in independent claim 1 as amended and Singh *et al.* '706 and Arita fail to overcome the deficiencies of Singh *et al.* '422 and, therefore, can not teach or suggest all limitations of claims that depend there from. Accordingly, withdrawal of this rejection and allowance of the claims is requested.

Claims 18-23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Singh *et al.* '422 further in view of Singh *et al.* '706 as applied to claim 17as amended above, and further in view of Arita. This rejection should be withdrawn for at least the following reasons. None of the cited references, alone or in combination, teach or suggest all limitations recited in the subject claims.

Claims 18-23 depend from independent claim 17. As discussed above, Singh *et al.* '422 does not teach or suggest all limitations recited in amended independent claim 17 and Singh *et al.* '706 and Arita fail to overcome the deficiencies of Singh *et al.* '422 and, therefore, can not teach or suggest all limitations of claims that depend there from. Withdrawal of this rejection and allowance of the claims is respectfully requested.

II. Rejection of Claims 9, 11-16 Under 35 U.S.C. §103(a)

Claims 9 and 11-16 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. 6,650,422 (Singh *et al.* '422) in view of U.S. 6,561,706 (Singh *et al.* '706) and US 6,905,949 (Arita) as applied to claims 1-8, 10 and 17-23 above, and further in view of U.S. 6,730,458 (Kim, *et al.*). Withdrawal of this rejection is respectfully requested for at least the following reasons. Neither Singh *et al.* '422 nor Singh *et al.* '706, Arita and Kim *et al.*, alone or in combination, teach or suggest all limitations recited in the subject claims.

Claim 9 depends from amended independent claim 1. Kim *et al.* does not make up for the aforementioned deficiencies of Singh *et al.* '422, Singh *et al.* '706 and Arita with respect to the independent claim 1 as amended. Kim *et al.* discloses that "exemplary embodiments of the invention provide methods for shrinking the size of contact hole by exposing an ArF resist pattern during thermal treatment at a temperature between about 30.degree. C. and about 180.degree. C. to VUV light energy or E-beam energy to cause the resist pattern to flow in a controllable and reproducible manner. This patterning method thereby provides the ability to reduce the patterned opening sizing in fine resist patterns while improving CD stability and reproducibility to enhance the process yield and the reliability of the resulting semiconductor devices." (*See* col. 3, lines 42-51). Kim *et al.* develops the exposed photoresist layer to form the first resist pattern and then exposes the first pattern to VUV energy to flow the first pattern to form a second pattern. (*See* col. 7, lines 25-30, Fig. 6). Hence, Kim *et al.* like Arita performs a *secondary operation on the semiconductor, whether or not it is necessary,* whereas the claimed

invention ***monitors line-edge roughness and critical dimension to determine if adjustments are necessary***. Also, Kim *et al.* is silent with respect to monitoring line-edge roughness. Hence, Singh *et al.* '422, Singh *et al.* '706, Arita and Kim, *et al.*, alone or in combination, fail to teach or suggest all limitations recited in the subject claims. Accordingly, this rejection should be withdrawn.

Claims 11-16 depend from independent claim 10. Kim *et al.* does not make up for the aforementioned deficiencies of Singh *et al.* '422, Singh *et al.* '706 and Arita with respect to the independent claim 10. This rejection should be withdrawn for at least the following reasons. Singh *et al.* '422, Singh *et al.* '706, Arita and Kim, *et al.* alone or in combination, do not teach or suggest all of the limitations recited in the subject claims. Claim 10 discloses a method for mitigating line-edge roughness on a semiconductor device by determining ***whether line-edge roughness exists on a patterned photoresist, employing a non-lithographic shrink technique to mitigate line-edge roughness and employing a trim etch technique to compensate for any increase in critical dimension*** between lines on a photoresist. Kim *et al.* is a method for reducing the size of pattern features through post-development processing. (*See* col. 1, lines 10-12). As discussed *supra* Kim *el al.* performs the post-developing process whether or not it is necessary, whereas the claimed invention monitors line edge roughness and critical dimension to determine if secondary operations are needed. In addition, Kim et al. does not disclose determining whether line edge roughness is extant and if it is, mitigating the roughness.

Claims 11-16 depend from independent claim 10. As discussed above, Singh *et al.* '422 does not teach or suggest all limitations recited in independent claim 10 and Singh *et al.* '706, Arita and Kim, *et al.* fail to overcome the deficiencies of Singh *et al.* '422 and, therefore, can not teach or suggest all limitations of claims that depend there from. Therefore, withdrawal of this rejection and allowance of the claims is respectfully requested.

CONCLUSION

The present application is believed to be in condition for allowance in view of the above comments and amendments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063[AMDP981US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

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